**generate bitstream & load with pynq**

After done modifying an bd (vivado block design), you can click on generate bitstream (left). If asked about “synthesis is out-of-date”, click yes (right):

|  |  |
| --- | --- |
|  |  |
|  |  |

Once done (would take roughly an hour), export the hardware as .xsa file. First click Export Hardware from the menu (left), a window will pop out. Click next, then select include bitstream, then click next (right). Then give the file a name and location to export to, then click next, then click finish:

|  |  |
| --- | --- |
|  |  |

To load into fpga with pynq, you first extract the .xsa with, e.g., 7-zip (left). In the extracted file, search for the .hwh file with same name as the bd in vivado, and a .bit file (right), then make the name of both (excluding extension) the same, e.g., d\_1.hwh and d\_1.bit.

|  |  |
| --- | --- |
|  |  |

Next, drag and drop d\_1.hwh and d\_1.bit into jupyterLab (left), then run the codes to load the bitstream into fpga (right). The qick\_path is the directory where you place the downloaded qick repository.

|  |  |
| --- | --- |
|  |  |